Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 19, with the following amended paragraph:

These new assembly techniques are low-cost but have the disadvantage that the on-glass wiring track resistance is much higher than the track resistances found on printed circuit boards. The sheet resistance for the on glass interconnection is 100 times higher, than for the PCB-technique. This difference is due to the fact that PCB conductors are thicker and use ~~low-resistively~~ low-resistivity material, i.e. laminated copper around 35-µm thick, compared to on-glass conductors, which ~~uses usually~~usually use vapour-deposited Al around 0.2-µm thickness. Typical values for the track resistance between two gate drivers are 25Ω for the gate off supply track and up to 100Ω for tracks of other signals. The gate off supply track (VL) supplies the OFF state voltage of the gate lines, it holds the TFT-transistors of the non-addressed lines in the non-conducting (OFF) state.

Please replace the paragraph beginning on page 7, line 22, with the following amended paragraph:

The capacitor Clc is the ~~capacity~~capacitor of the liquid crystal cell. Cst' is a simplification of the storage capacitor Cst in parallel with Cc, which is the overlap capacitance between Gly-1 and dot. ~~Capacity~~ Capacitor Csgo is the overlap capacitance between source line SLx and gate line GLy. Rg1 is the gate line resistance per dot. ~~Example of typical values is~~Examples of typical values are: Clc=250 fF, Cst=175 fF, Cc=18 fF-> Cst'=193 fF, Csgo=19 fF, Rg1=1Ω, Cg1=109 fF.

Please replace the paragraph beginning on page 8, line 31, with the following amended paragraph:

FIG. 5a shows the schematic diagram of the capacitive coupling from source lines SL into gate lines GL. Due to the column to row overlap capacitance Csgo in every dot,

this 4.5V jump of the average column voltage is capacitively coupled into all the gate lines Gly of the LCD-panel. The capacitance Cg1 is the simplification of the ~~capacities~~ capacitors Cst' and Clc, as described in FIG. 2. The ratio between the ~~capacity~~ capacitor Csgo and ~~capacity~~ capacitor Cg1 is roughly 1:5. This means that about 1/6 of the amplitude of the pulse present on the source lines is coupled into the gate lines GL. Looking at a pair of TFT-LC cells, source line SLodd and source line SLeven can be replaced by the average (SLodd+SLeven)/2, which is represented in FIG. 5b. So the capacitive coupled voltage into the gate lines will be in this example 4.5V/6=750 mV. Note that the pulses SLodd and SLeven are out of phase because the polarity of the applied voltage is opposite for two adjacent columns, due to the dot inversion drive scheme.

Please replace the paragraph beginning on page 9, line 31, with the following amended paragraph:

FIG. 8 shows a sampling of dot voltage. At the sampling point tsample, the voltage at the source line SLx is sampled on the dot. A voltage V.sub.GLy-1 different from the ideal VL value results in an extra charge on the dot, which is preserved on the ~~capacities Cst~~capacitors Cst' and Clc, once the TFT transistor is off. Since the mean voltage on GLy-1 is VL, the mean voltage on the dot cell gets an offset voltage of $\Delta Vdot=-(VLy-1(t_{sample})-VL)*Cst'/(Cst'+Clc)$.

Please replace the paragraph beginning on page 10, line 5, with the following amended paragraph:

Since Cst and Clc are about the same, the mean dot voltage has an offset (error) of approximately half the voltage $VL_{y-1}-VL$ at the sampling moment. Because the disturbance on V_{GLy-1} is equal to the disturbance of the local VL_1 to VL_3 lines at the input of the gate drivers, the error in the dots depends on the local VL disturbance. Because the VL track resistance ~~increased~~ increases in finite steps from gate driver to gate driver, the dot error voltage $\Delta Vdot$ also makes a step at the boundary between two

gate drivers. This step in the error function can be detected by the eye and is showed in FIG. 3. The visible result is a horizontal block-dim with grey shades of different intensity and with edges corresponding to the boundary of every gate driver device.

Please replace the paragraph beginning on page 11, line 3, with the following amended paragraph:

FIG. 10 shows a LCD-panel with additional supply track ~~Vlclean~~VLclean, wherein the gate drivers GD 1 -GD3 are illustrated schematically. The main problem with the DODO pattern is that the local supplies of the gate driver devices (VL_1, VL_2, VL_3, etc.) do not recover fast enough from the coupling of the source lines. The time constant is much too long due to the large LCD-panel resistance and the large sum of the LCD-panel gate line capacitance. This time constant can practically not be reduced. However, the VL error voltage has only a detrimental effect to the storage capacitors of the addressed line of the LCD-panel at sampling point. Whether the non-addressed lines have their ~~capacity~~capacitor Cst reference voltage jumping around from line to line is only of second importance, since it does not alter the sampling operation of the dots. The present invention is based on this singular observation: only the presently addressed line needs a clean or error-less VL line connected to ~~capacity~~capacitor Cst in order to store the correct dot voltage at sampling point.

Please replace the paragraph beginning on page 11, line 29, with the following amended paragraph:

FIG. 11b shows the output stage architecture of a gate driver with 2 gates off VL supplies. Instead of one PMOS MP1 and one NMOS transistor MN1, there is one PMOS MP1 and 2 ~~NMOST~~ NMOS (MN1 and MN2) for the gate driver with additional ~~Vlclean~~ VLclean line. In the output stage with additional VLclean line, the timing for MP1 remains the same as with traditional gate drivers. MN1 and MN2 are however driven slightly ~~differently~~different. As depicted in FIG. 12, MN2 is conducting during the whole phase GLy-1, so the gate line GLy-1 is connected to VLclean line when gate line GLy is

selected. MN1 is conducting in all other unselected phases, so all other gate lines are connected to VL. Note that it is recommended to turn-on MN1 already at the end of phase GLy when OUTx switches from VH to VL. This transition, which determines the sampling point (tsample) is usually induced by activating signal DIS ("disable") or EON ("output enable not").